AMENDMENTS TO THE CLAIMS

1. (Currently amended) A cell that is ~~can be~~ used as a dynamic memory cell for storing data or a field programmable gate array (FPGA) cell for programming, the cell useful in an array having column bitlines, read bitlines, and row wordlines, the cell comprising:

a capacitor having a first terminal and a second terminal, the first terminal connected to a column bitline, said second terminal connected to a switch control node;

a select transistor having a gate, a source, and a drain, said gate connected to said ~~write~~read bitline, said source connected to said switch control node, and said drain connected to a row wordline; and

a switch being controlled by said switch control node, wherein said switch control node stores data as a voltage indicative of a one or a zero.

2. (original) The cell of Claim 1 wherein said switch is a MOSFET and a gate of said MOSFET being connected to said switch control node.

3. (original) The cell of Claim 1 wherein data is placed onto said switch control node by turning on said select transistor and placing the data onto said row wordline.

4. (original) The cell of Claim 1 wherein said first terminal of said capacitor, said gate of said select transistor and a gate of said switch is formed from the same layer of polysilicon.

5. (original) A method of operating a dual mode cell that is connected to a row wordline, a column write bitline, a read bitline, said cell comprising a capacitor having a first terminal and a second terminal, the first terminal connected to said column write bitline, said second terminal connected to a switch control node, a select transistor having a gate, a source, and a drain, said gate connected to said read bitline, said source connected to said switch control node, and said drain connected to a row wordline, and a switch being controlled by said switch control node, the method comprising:

when said cell is operating as a field programmable gate array (FPGA) cell and is to be programmed,

(1) applying a first voltage to said column bitline;

(2) turning on said select transistor; and

(3) applying a second voltage to a selected one of the row wordlines, wherein the first voltage and the second voltage form a potential difference across said capacitor to break down a dielectric of said capacitor converting said capacitor into a resistive device;

when said cell is operating as a dynamic memory cell to store data,

(1) turning on said select transistor;

(2) applying said data to said switch control node through said row wordline, wherein said switch control node stores said data as a voltage indicative of a one or a zero.

6. (original) The method of Claim 5 further including periodically refreshing said data when said cell is operating as a dynamic memory cell.

7. (original) The method of Claim 5 wherein said select transistor is turned off before the data on said row wordline is removed.

8. (Currently amended) A cell that ~~can~~is ~~be~~ used as a dynamic memory cell for storing data or a field programmable gate array (FPGA) cell for programming, the cell useful in an array having column bitlines, write ~~read~~ bitlines, and row wordlines, the cell comprising:

a capacitor having a first terminal and a second terminal, the first terminal connected to a column bitline (Bp), said second terminal connected to a switch control node;

a select transistor having a gate, a source, and a drain, said gate connected to said write bitline (Bw), said source connected to said switch control node, and said drain connected to a row wordline (WL);

a switch being controlled by said switch control node, wherein said switch control node stores data as a voltage indicative of a one or a zero;

a sense device for determining the voltage on said switch control node.

9. (original) The cell of Claim 8 wherein said switch is a MOSFET and a gate of said MOSFET being connected to said switch control node.

10. (original) The cell of Claim 8 wherein data is placed onto said switch control node by turning on said select transistor and placing the data onto said row wordline.

11. (original) The cell of Claim 8 wherein said first terminal of said capacitor, said gate of said select transistor and a gate of said switch is formed from the same layer of polysilicon.

12. (original) The cell of Claim 8 wherein the sense device is a transistor having its gate connected to said switch control node and its drain connected to a sense bitline (Bs) and its source connected the said wordline (WL).

13. (original) The cell of Claim 12 further including a diode connected in series to said sense device and between said row wordline and said sense bitline.

14. (Currently amended) A cell that ~~can~~is ~~be~~ used as a dynamic memory cell for storing data, the cell useful in an array having column bitlines, ~~read~~ write bitlines, and row wordlines, the cell comprising:

a capacitor having a first terminal and a second terminal, the first terminal connected to a column bitline (Bp), said second terminal connected to a switch control node, said switch control node storing said data;

a select transistor (Tw) having a gate, a source, and a drain, said gate connected to said write bitline (Bw), said source connected to said switch control node, and said drain connected to a row wordline; and

a sense device for determining the data on said switch control node.

15. (original) The cell of Claim 14 wherein data is placed onto said switch control node by turning on said select transistor and placing the data onto said row wordline.

16. (original) The cell of Claim 14 wherein said first terminal of said capacitor, said gate of said select transistor and a gate of said switch is formed from the same layer of polysilicon.

17. (original) The cell of Claim 14 wherein the sense device is a transistor having its gate connected to said switch control node and its drain connected to a sense bitline (Bs).

18. (original) The cell of Claim 17 further including a diode connected in series to said sense device and between said row wordline and said sense bitline.